IN THE SPECIFICATION:

Please amend the specification as follows:

Paragraph 72 (p. 22):

The counter ~~2001~~ 2002 stores a pointer ptr_o that points to and controls the amount of delay to be implemented by the programmable delay 2001. Pointer ptr_o may be incremented, decremented, or maintained at a constant value, in accordance with commands from the phase comparator 2003. Pointer ptr_o may also be reset in accordance with signal rst_n, and a new value of ptr_o may be loaded from signal ptr_i when signal ldptr is set. When the counter ~~2001~~ 2002 changes the output of ptr_o, some of the bits of ptr_o may not change exactly simultaneously, possibly resulting in a glitch at the control input of the multiplexor 2103 in the programmable delay 2001 (and thus in dpa_o). A Gray counter could be used if desired to avoid such glitches, since in Gray counters only one bit at a time changes. However, such glitches are inconsequential in this embodiment since they would occur just after the rising/active transition edges of clock CKR, and in the current embodiment dpa_o is read only on the falling/inactive transition edges, allowing ptr_o half a period to stabilize. Thus, a Gray counter would not be necessary.

Paragraph 73 (p. 22):

Referring to Figure 23, the phase comparator 2003 may include a phase alignment detection (PHAD) block 2301, which analyzes sequences of commands affecting ptr to decide whether dpa_o is synchronized. The phase comparator 2003 may further include an analyzer 2302 that provides information to a decision block 2304 that enables the decision block 2304 to make intermediate decisions as to whether the pointer ptr stored in the counter ~~2001~~ 2002 should be incremented, decremented, or maintained at a constant value.

Paragraph 76 (p. 23):

Figure 26 illustrates a finite state machine 2600 that may be implemented by the PHAD block 2301 to control the illustrative two bit phok counter. The finite state machine 2600 as shown has a plurality of states x and s0 through s8. From all of these states, if a no action command is sensed (or if there is no increment or decrement command), then the state remains unchanged, with two exceptions that will be mentioned below. State x is an initialization state in which the phok counter is reset. Next, at state s0, if the PHAD block 2301 senses either a decrement command or an increment command, then the finite state machine 2600 goes to either state s1 or state s2, respectively. From state s1, if an increment command is sensed, then state s5 is entered and the phok counter is incremented, and if a decrement command is sensed, then state s3 is entered. Oppositely, from state ~~d2~~s2, if a decrement command is sensed, then state s6 is entered and the phok counter is incremented, and if an increment command is sensed then state s4 is entered. In other words, only a series of two opposite commands (decrement, then increment; or increment, then decrement) will cause the phok counter to be incremented at this point. Assuming that this has happened, then at state s5 if a decrement command is sensed, then state s6 is entered and the phok counter is incremented. Oppositely, at state s6 if an increment command is sensed, then state s5 is entered and the phok counter is incremented. Thus, each time a decrement-increment or increment-decrement series of adjacent commands is sensed, the phok counter is incremented.

Paragraph 85 (p. 29):

An illustrative status format (where stssel is set to zero) is shown in Figure 35, supplemented with an explanation of ~~the~~ each portion of the status format in Table 9.